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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,470	03/29/2001	Yoshihiro Yoneda	82-01	5656

7590 08/12/2002

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

EXHIBIT "A"

UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, DC 20231
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Paper No.

Notice of Non-Compliant Amendment (37 CFR 1.121)

The amendment filed on 7/30/02 is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121, as amended on September 8, 2000 (see *65 Fed. Reg. 54603*, Sept. 8, 2000, and *1238 O.G. 77*, Sept. 19, 2000). In order for the amendment to be compliant, applicant must supply the following omissions or corrections in response to this notice.

THE FOLLOWING ITEMS ARE REQUIRED FOR COMPLIANCE WITH RULE 1.121 (APPLICANT NEED NOT RE-SUBMIT THE ENTIRE AMENDMENT):

☐ 1. A clean version of the replacement paragraph(s)/section(s) is required. See 37 CFR 1.121(b)(1)(ii).

☒ 2. A marked-up version of the replacement paragraph(s)/section(s) is required. See 37 CFR 1.121(b)(1)(iii).

☐ 3. A clean version of the amended claim(s) is required. See 37 CFR 1.121(c)(1)(i).

☐ 4. A marked-up version of the amended claim(s) is required. See 37 CFR 1.121(c)(1)(ii).

Explanation: _____

_____

(LIE: Please provide specific details for correction to assist the applicant. For example, "the clean version of claim 6 is missing.")

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714 and the USPTO website at http://www.uspto.gov/web/offices/dcom/olia/pbg/sampleaf.pdf. **A condensed version of a sample amendment format is attached.**

☐ **PRELIMINARY AMENDMENT:** Unless applicant **supplies the omission or correction** to the preliminary amendment in compliance with revised 37 CFR 1.121 noted above within ONE MONTH of the mail date of this letter, examination on the merits may commence without entry of the originally proposed preliminary amendment. This notice is not an action under 35 U.S.C. 132, and this ONE MONTH time limit is not extendable.

☒ **AMENDMENT AFTER NON-FINAL ACTION:** Since the above-mentioned reply appears to be *bona fide*, applicant is given a TIME PERIOD of ONE MONTH or THIRTY DAYS from the mailing of this notice, whichever is longer, within which to **supply the omission or correction noted above** in order to avoid abandonment. EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136(a).

MS. McMillan
Legal Instruments Examiner (LIE)
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(Rev. 12/01)

Application
of: Yoshihiro Yoneda
Serial No.: 09/820,470
Filed: March 29, 2001
For: SURFACE-MOUNTING SUBSTRATE AND STRUCTURE COMPRISING SUBSTRATE AND PART MOUNTED ON THE SUBSTRATE
Atty Doc. No. 082-01
Order No. 0744
Atty: JJS
Date: July 26, 2002
The Patent and Trademark Office is respectfully requested to place its Stamp on this POSTAL CARD and place it in the outgoing mail.

The following papers have been received:

1) This cover letter;
2) Amendment (12 pages);
3) Replacement spec. marked up and clean pages (4 pages)
4) Substitute formal drawings (18 sheets - Figs. 1-25C);
5) Marked up drawings (18 sheets);
6) Extension fee of $110;
7) Postcard ~~to be~~ return receipt.

Respectfully Submitted
John J. Simkanich

CERTIFICATE OF FIRST CLASS
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Exhibit "B"

SURFACE-MOUNTING SUBSTRATE AND STRUCTURE COMPRISING SUBSTRATE AND PART MOUNTED ON THE SUBSTRATE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a surface-mounting substrate for mounting thereon a part, such as a semiconductor device, and a structure comprising a substrate and a part surface-mounted thereon.

2. Description of the Related Art

As a substrate for mounting thereon a part, such as a semiconductor device, there have been provided a product having a laminate structure of an insulation layer(s) and a patterned wiring line layer(s) on at least a side of a core substrate.

Such a substrate is illustrated in Fig. 20, which is a plan view of a substrate for mounting a semiconductor device (not shown) by flip chip bonding, the substrate having connecting terminals 10 arranged on a surface of the substrate so as to be spaced from each other and to form an array of the terminals 10.

Fig. 21 illustrates a construction of the laminate structure of electrical insulation layers and patterned wiring line layers provided on a core substrate 20. The laminated structure comprises first and second inner wiring line layers 12a, 12b, and an outermost wiring line layer 12, which are formed so as to have certain patterns. The first inner wiring line layer 12a is provided on a side of the core substrate 20, and the second inner layer 12b and the outermost wiring layer 12 are separated from the first inner layer 24a and the second inner layer 24b by insulation layers 22a and 22b, respectively. The wiring lines in the adjacent layers are connected to each other by vias 12a, 12b which are formed in the respective insulation layers 22a, 22b. A through hole 26 is formed in the core substrate 20, and

effectively employed for substrates having connecting terminals arranged at a small pitch of, for instance, 100 micrometers or less.

However, when the connecting terminals 10 are arranged with a smaller gap, such as about 30 micrometers, a problem that solder materials on adjacent terminals 10 form bridges when they are fused in a reflow process, resulting in short-circuit between the adjacent terminals 10, arises. Fig. 22 illustrates a mounting substrate having a bridge structure 14a of solder materials on the adjacent connecting terminals 10, which is formed during a reflow process. In conventional surface-mounting substrates, the side faces of the connecting terminal 10 are exposed, and the solder material 14 provided on the top surface of the terminal 10 can be coated not only to the top surface of the terminal 10 but also to the exposed side faces thereof during a reflow process. Short-circuits between the adjacent terminals 10 due to such bridge structures of solder materials tend to occur when the space between adjacent terminals 10 becomes smaller.

In addition, conventional surface-mounting substrates also have a problem that variation in the thicknesses (heights) of the connecting terminals 10 causes variation in the amounts of solder materials on the terminals 10, which in turn causes variation in the heights of the solder materials after coated to the terminals 10.

These problems cannot be overlooked in order to provide a miniaturized semiconductor product having an increased number of pins by which the product is to be mounted on a substrate.

Conventional surface-mounting substrates further have a problem that inner layers of patterned wiring lines in a build-up structure are designed based only on wiring schemes, line widths, and line gaps in the respective layers, without considering densities of lines